IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method comprising:

configuring a plurality of heterogeneous processing elements in a heterogeneous reconfigurable device, the plurality of heterogeneous processing elements being coupled to a plurality of routers, the plurality of routers being interconnected by a plurality of mesh interconnect networks, the plurality of mesh interconnect networks being allocable to either data or control or a combination thereof; and

allocating [[a]] the plurality of mesh interconnect networks for data and control in [[a]] the heterogeneous reconfigurable device.

2. (Currently Amended) The method of claim 1 further comprising:

reading a protocol file from a memory; and

configuring [[a]] the plurality of heterogeneous processing elements with information in the protocol file;

wherein the protocol file includes allocation information for the plurality of mesh interconnect networks.

3. (Currently Amended) The method of claim 1 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises dedicating the first plane to control and dedicating the second plane to data.

4. (Original) The method of claim 3 further comprising re-allocating the first plane to be shared between data and control.

5. (Currently Amended) The method of claim 1 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises allocating the first plane to be shared between data and control.

6. (Currently Amended) The method of claim 1 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises allocating both the first plane and the second plane to be shared between data and control.

7. (Currently Amended) A method comprising:

translating a design description into a configuration for a plurality of heterogeneous processing elements coupled to routers interconnected by a plurality of mesh interconnect networks, the plurality of mesh interconnect networks being allocable to either data or control or a combination thereof; and

allocating [[a]] the plurality of mesh interconnect networks between data and control.

8. (Original) The method of claim 7 wherein allocating comprises determining whether latency constraints can be met with a shared data and control mesh network.

9. (Original) The method of claim 7 wherein translating and allocating results in a protocol file, the method further comprising storing the protocol file in a memory.

10. (Original) The method of claim 9 further comprising translating a second design description and performing a second allocation, resulting in a second protocol file, and storing the second protocol file in the memory.

11. (Currently Amended) An apparatus including a medium to hold machine-accessible instructions that when accessed result in a machine performing:

configuring a plurality of heterogeneous processing elements in a heterogeneous reconfigurable device, the plurality of heterogeneous processing elements being coupled to a plurality of routers, the plurality of routers being interconnected by a plurality of mesh interconnect networks, the plurality of mesh interconnect networks being allocable to either data or control or a combination thereof; and

allocating [[a]] the plurality of mesh interconnect networks for data and control in [[a]] the heterogeneous reconfigurable device.

12. (Currently Amended) The apparatus of claim 11 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises dedicating the first plane to control and dedicating the second plane to data.

13. (Original) The apparatus of claim 12 further comprising re-allocating the first plane to be shared between data and control.

14. (Currently Amended) The apparatus of claim 11 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises allocating the first plane to be shared between data and control.

15. (Currently Amended) An apparatus comprising:

a heterogeneous network of processing elements; and

first and second mesh interconnect networks coupled to the heterogeneous network of processing elements, wherein the apparatus is programmable to utilize the first and second mesh interconnect networks for any combination of data and control.

16. (Currently Amended) The apparatus of claim 15 further comprising a processor to dynamically allocate the first and second mesh interconnect networks between data and control.

17. (Currently Amended) The apparatus of claim 15 wherein the heterogeneous network of processing elements are configurable to communicate over the first and second mesh interconnect networks using packets of information.

18. (Currently Amended) The apparatus of claim 15 wherein the heterogeneous network of processing elements is configurable to utilize the first mesh interconnect network for data communication and the second mesh interconnect network for control communication.

19. (Currently Amended) The apparatus of claim 18 wherein the heterogeneous network of processing elements is configurable to utilize the first mesh interconnect network for data communication and the second mesh interconnect network for both data and control communication.

20. (Currently Amended) The apparatus of claim 18 wherein the heterogeneous network of processing elements is configurable to utilize both the first and second mesh interconnect networks for both data and control communication.

21-30. (Canceled)